ACCURATE DESIGN CENTERING AND YIELD PREDICTION USING THE "TRUTH MODEL"

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ABSTRACT

The "Truth Model" is introduced as the first implementation of a statistically validated GaAs FET simulation model. In this paper we examine the power and accuracy of the Truth Model by comparing the predicted and measured statistical response of a GaAs MMIC 0.5 - 2.5 Ghz amplifier. By design centering a small-signal amplifier both with and without the use of the Truth Model, we show that not only yield estimates are affected by the accuracy of the device statistical model, but also the design center.
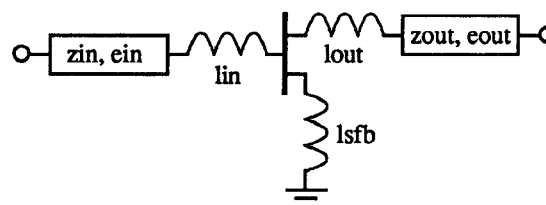
I. INTRODUCTION

In a previous work, it was illustrated that "low-order" statistical models of the measured GaAs FET data are not sufficient to faithfully reproduce the measured low-order S-parameter statistics [1, 2]. The authors of [2] proposed a solution to this problem where the original measured FET (or S-parameter) data is retained as the statistical model for the device. They termed this implementation the "Truth Model", because the Joint Probability Density Function (JPDF) based on the measured data sample is the *reference* by which any proposed statistical model will be judged [3]. Independently, workers at TRW found empirically that the Truth Model was capable of higher predictive power such that closer agreement between measured and modeled response data was observed [4].

In this paper we examine the power and accuracy of the Truth Model in two ways. First by design centering a small-signal amplifier both with and without the use of the Truth Model, we show that not only yield estimates are affected by the accuracy of the device statistical model, but also the design center. Then we compare the predicted and measured statistical response of a GaAs MMIC 0.5 - 2.5 Ghz amplifier.

II. DESIGN CENTERING WITH THE TRUTH MODEL

The following example is taken from Purviance, *et al* [5]. The circuit and optimization specifications for this example are given in Figure 1. Starting from the nominally optimized component values as given in [5], design centering using Touchstone™ [6] was performed twice using the following assumptions on the FET model statistics: 1) use the Truth Model, and 2) use the low-order statistical model where the distributions and pairwise correlations are identical to that of the measured data [1, 2]. The designable parameters are zin, zout, ein, eout, lin, lout, lsfb, and these are modeled as independent uniform variables with ±10% tolerance limits.

Optimization SPECS			
	S11	S22	S21
Nominal	<-10dB	<-10dB	=15dB
Yield	<-8dB	<-8dB	<16, >14dB

Figure 1   Single FET 3.8 - 4.2 Ghz Amplifier used in the Design Centering Example.

Tables 1 and 2 summarize the results of this centering exercise. Table 1 shows yield estimate results (using a 5000 trial Monte Carlo analysis). Note that yield is improved using both the low-order FET statistical model (31.4%-48.5%) and the Truth Model (31.4%-58.5%). However, we should point out that the designer using the Truth Model can have higher confidence that his design will be both reliable and producible. Another important result here is that both the yield estimate and the design center (Table 2) are affected by the accuracy of the device statistics.

In the following section we investigate the predictive powers of the Truth Model in an effort to verify it's statistical accuracy.

III. STATISTICAL RESPONSE PREDICTION WITH THE TRUTH MODEL

A 0.5 to 2.5 GHz feedback amplifier has been designed using two 0.5 X 300 micron FETs [7]. The amplifier is intended to be a drop-in replacement for an existing hybrid amplifier and, as such requires excellent gain flatness and low dc bias current. The single stage gain needs to be greater than 13.5 dB and a low noise figure is not required. To ensure ease of integration at the system level, the VSWR must be better than 2:1 out to 6 GHz. To reduce assembly costs and verify the circuit performance on-wafer, all bias circuitry was included on the chip. Figure 2 shows the schematic diagram of the MMIC amplifier.

Design	Parameter Assumption for Yield Analysis	Yield Estimate Before Centering	After Centering
1	Distributed-correlated	44.6%	57.5%
1	Truth Model	31.4%	48.5%
2	Distributed-correlated	44.6%	46.2%
2	Truth Model	31.4%	58.5%
NOTE: Design 1 -> design centered using Distributed-Correlated FET stats, Design 2 -> design centered using the TRUTH MODEL			

Table 1   Yield estimates before and after design centering.

Parameter	Univariate characterization	Multivariate characterization	Delta %
zin	35.52 Ω	38.15 Ω	7.87
ein	83.78 deg	84.97 deg	1.42
lin	3.21 nH	3.23 nH	2.43
lsfb	0.55 nH	0.57 nH	4.56
lout	7.88 nH	8.48 nH	7.56
zout	82.07 Ω	86.05 Ω	4.85
eout	93.60 deg	99.80 deg	6.62

Table 2   Design centering results for the single FET amplifier.

Circuit Design. A feedback topology was chosen in order to provide flat gain over the wide bandwidth. The gate periphery was optimized to deliver the necessary output power at the required bias condition. The small signal FET performance was calculated from an equivalent circuit model. The model's values were derived from on-wafer measured S-parameters of test FETs. The S-parameters are measured for every wafer processed at Watkins-Johnson Company (W-J) and a database is used to arrive at a statistically significant model. A lossy match is used on both the input and output to achieve good VSWR over the complete frequency range. The spirals were taken from a library of characterized elements and are represented in the circuit design by their measured S-parameters.
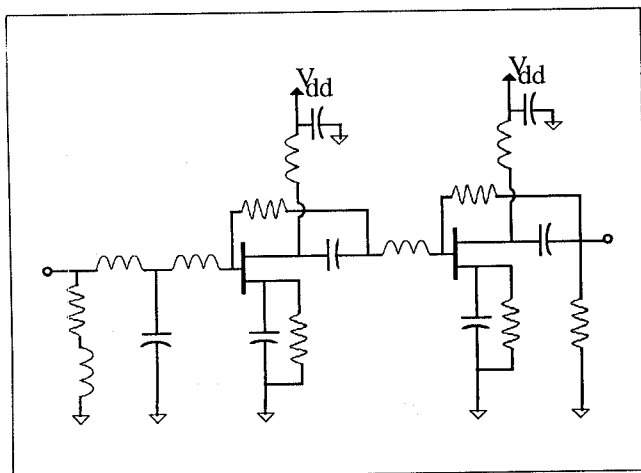

Figure 2   Schematic diagram of the 0.5 - 2.5 Ghz MMIC Amplifier.

Circuit Fabrication. The amplifier chips are fabricated using W-J's 0.5 micron MMIC process. Ion implanted wafers are used with a peak carrier concentration in the channel layer of 4.0×10^{17} cm^{-3}. Device isolation is achieved using an oxygen implant. Ohmic contacts are formed from an Ni/Au/Ge metallization. Silicon nitride serves as both the capacitor dielectric and the chip passivation. Precise resistor values are realized using TiWN thin film resistors. Electroplating of air bridges and transmission lines completes the front side processing. The substrates are lapped to a thickness of 110 microns and vias are laser drilled from the back side. Following chip separation the fabrication is complete. The final chip size is 2.1 X 1.5 X 0.1 mm. Figure 3 shows a picture of the MMIC.

Circuit Statistical Response Performance. Turn-on performance showed the amplifier to be a first pass design success. The measured and simulated statistical response plots are shown in Figures 4 and 5, respectively. A nominal gain of 14.5 ± 0.2 dB from 0.5 to 2.5 GHz was measured using the Cascade Microtech wafer probe. The input and output VSWR was measured to be better than 1.7:1 across the band. Except for the very low end of the band, the input VSWR is typically better than 1.35:1 and the output VSWR better than 1.25:1. These numbers are averages from the first two lots of wafers. The amplifier's performance has been reproducible from wafer to wafer and wafer lot to wafer lot. Chips measured in a test fixture have shown excellent correlation to the on-wafer rf data. The amplifier uses less than 80 mA of bias current at 5 V.
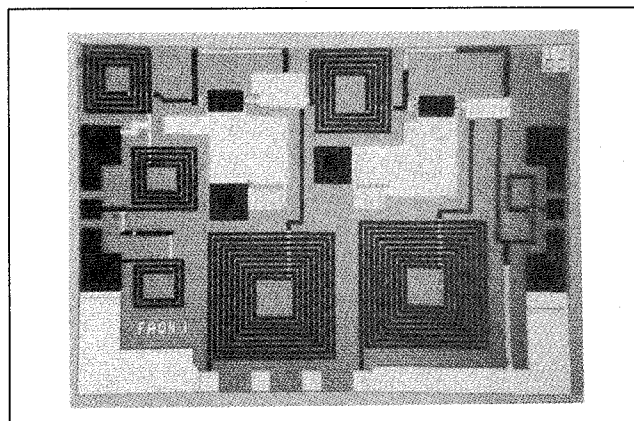

Figure 3   Photograph of the 0.5 - 2.5 Ghz MMIC Amplifier.

IV. CONCLUSIONS

The first comprehensive demonstration of the Truth Model as a statistically valid GaAs FET simulation model has been made. We have shown that design centering with low-order statistical models (distributions and correlations) can lead to uncertain and suboptimal results. Finally, we have illustrated the excellent predictive power of the Truth Model by showing close agreement between the measured and simulated statistical response of a 0.5 - 2.5 Ghz GaAs MMIC amplifier.

Application of the Truth Model concept is not restricted to device type or even for active devices. In any situation where complex high-order statistical relationships exist, the Truth Model will find utility. Additionally, the Truth Model should be regarded as the standard by which any proposed statistical model is measured. That is, *multivariate* moment equivalence should exist between any proposed model and the Truth Model measured data.

1202

Figure 4   Measured Statistical Response of the 0.5 - 2.5 Ghz MMIC Amplifier.
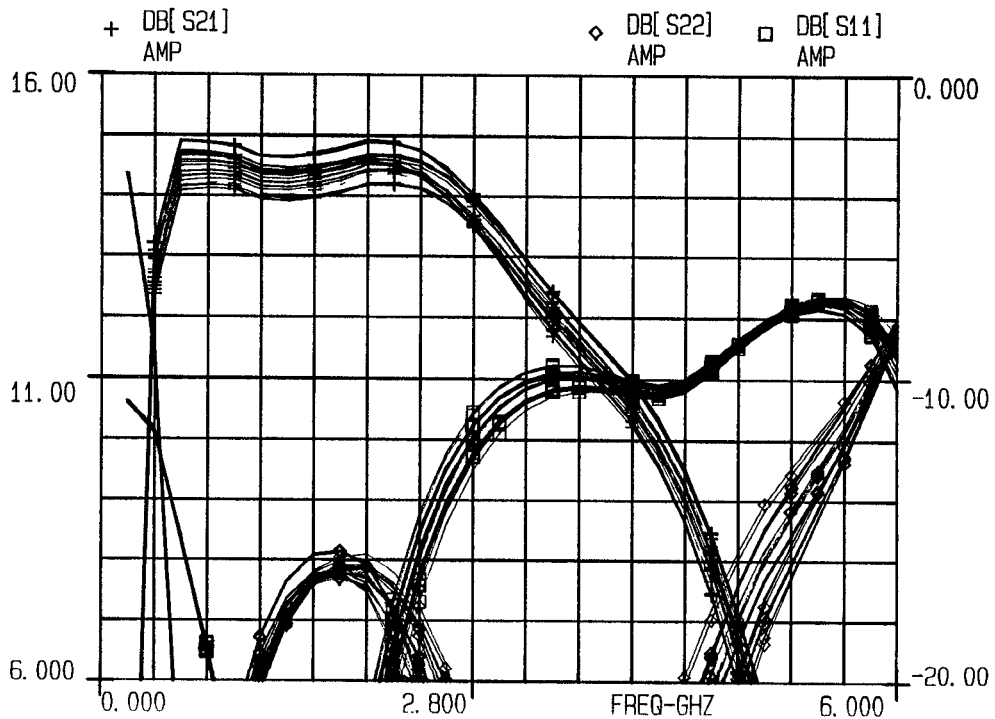
Figure 5   Simulated Statistical Response of the 0.5 - 2.5 Ghz MMIC Amplifier.

REFERENCES

(1)   M.D. Meehan, D.M. Collins, "Investigation of the GaAs
        FET Model to Assess its Applicability to Design
        Centering and Yield Estimation," EEsof Internal
        Development Report, Dec. 1987.

(2)   J. Purviance, M.D. Meehan, and D.M. Collins,
        "Properties of FET Statistical Data Bases," Proceedings
        of the IEEE MTT-S International Microwave
        Symposium, Dallas, TX, pp. 567-570:May 1990.

(3)   M. Meehan, L. Campbell, "Statistical Techniques for
        Objective Characterization of Microwave Device
        Statistical Data," IEEE MTT-S International
        Microwave Symposium, Boston, MA, June 1991.

(4)   M. Mlinar, S. Andrews, Private communication,
        Aug. 1989.

(5)   J. Purviance, D. Criss and D. Monteith, "FET Model
        Statistics and their Effects on Design Centering and
        Yield Prediction for Microwave Amplifiers,"
        Proceedings of the IEEE MTT-S International
        Microwave Symposium, New York, NY, pp. 315-
        318:May 1988.

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